AS998/A

Power Management IC

Features

- Low start-up current 64uA (typ)
- Low running current 2mA (typ)
- Low power light load mode
- Low power standby when OV is activated
- Extended commercial operating temperature range to 0-105C
- On-board fixed frequency oscillator 100kHz (typ)
- Frequency randomizer to reduce EMC emissions
- Dedicated OV shutdown pin
- On-board voltage ramp compensation
- On-board current sense filtering
- Optional primary side regulation

Description

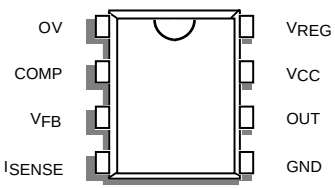
The AS998/AS998A is an IC intended for use as a PWM controller for switch mode power supplies. The device is particularly suited as a primary side controller for adapter, printer, peripheral, mobile chargers and desktop auxiliary power supplies. The AS998/AS998A is manufactured in BiCMOS technology and exhibits very low start-up and operating power. This allows the device to be suitable in applications where stringent standby or Blue Angel criteria are required.

Many of the external functions associated with PWM controllers have been integrated into the AS998/AS998A allowing the external component count to be significantly reduced. Features such as fixed internal oscillator, internal ramp compensation and current filters all reduce the external support components.

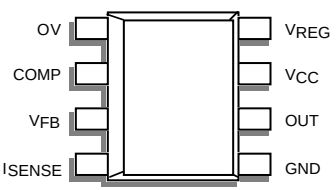
The AS998/AS998A has an output rise and fall time of 250/210 nS typical.

Pin Configuration — Top view

PDIP (N)



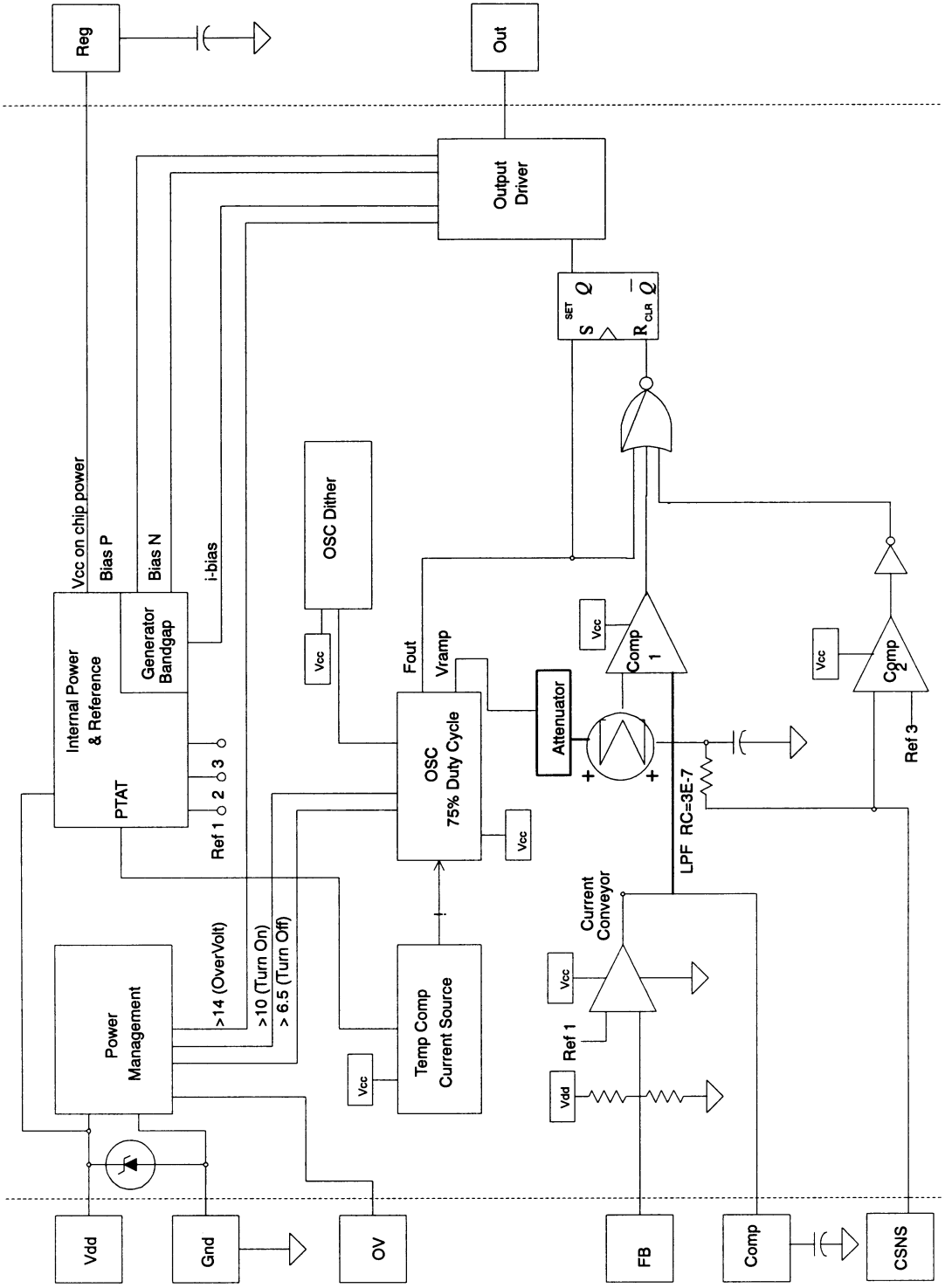
SOIC (D)



Ordering Information

Description	Temperature Range	Order Codes
AS998 8-Pin Plastic DIP	0 to 105° C	AS998N
AS998 8-Pin Plastic SOIC	0 to 105° C	AS998D
AS998A 8-Pin Plastic DIP	0 to 105° C	AS998AN
AS998A 8-Pin Plastic SOIC	0 to 105° C	AS998AD

Functional Block Diagram



Pin Descriptions

Pin #	LABEL	DESCRIPTION
1	OV	Overvoltage Pin. The OV input/output function is implemented by an on chip latch. This pin is driven to the Reg voltage if the on chip circuitry senses a VDD level greater than the OV threshold (VDDov). This error condition stops the part from generating any more output pulses until VDD has been reduced to the VDDul level and then raised as in a normal power-on sequence. Alternatively, the OV error condition can be cleared by forcing the OV pin to near ground. The output is immediately enabled following an OV clear function. The OV error condition can also be generated externally by temporarily forcing the OV pin to a voltage greater than the VOV threshold. This will force the part to latch an OV condition and not generate any more output pulses unless cleared as described.
2	COMP	Compensation Pin. This pin is the output of the error amplifier and can also be used as an input for an optocoupled control signal to the PWM comparator. Generally this pin is connected to a feedback network to FB. If an optocoupler feedback is used, COMP connects to the collector of the common emitter optocoupler, generally with a pull-up resistor to VDD or Reg.
3	FB	Feedback Pin. Inverting input to the error amplifier. This pin is tied to an internal default divider which will tend to regulate VDD at a nominal 11 V.
4	CSNS	Current Sense Input. The signal on this pin is fed via a low pass filter to the PWM comparator. Superimposed on the input to the PWM is a slope compensation ramp derived from the main oscillator. In addition to the above, the current sense signal is connected directly to an over-current comparator that detects an overload condition and immediately terminates the gate drive pulse with a minimum propagation delay.
5	GND	Circuit Common Ground.
6	OUT	Gate Drive Output. The current source and sink capability of the output buffer is tailored to minimize EMI. When the IC is not running, this pin is held low so a pull down resistor on the FET gate is not required.
7	VDD	Positive Supply Voltage. An on-board shunt regulator allows this IC to be powered via a simple resistor from a widely varying bias supply. The ICs power management block keeps the part in startup current mode while VDD is ramping up until the part turns on at the UVLhigh threshold. The IC then draws the specified supply current while operating unless VDD drops below the UVLlow threshold. If VDD drops below UVLlow, then the part will return to startup current mode.
8	REG	Voltage Regulator. Decoupling pin as required for internal low voltage supply. This pin may be used to source 1mA for the control opto coupler.

IC Block Diagram Description

POWER MANAGEMENT

This block contains reference generators and comparators to determine the under-voltage shutdown point, the power-on point, the primary regulation operating point, and the overvoltage shutdown point.

INTERNAL POWER / REFERENCE

This block includes a coarse regulator for on chip power and cascade voltages for HV circuitry, a bandgap for comparator references, a bias current generator, PTAT, BiasP and BiasN.

TEMPERATURE COMPENSATED CURRENT SOURCE

This block generates a constant current as a function of voltage and temperature with no off-chip components.

OSCILLATOR

Mirrored currents from the reference block are used to charge a capacitor to a threshold voltage at which point the direction is switched to an opposing 3X mirror to drive the capacitor to a lower limit threshold value. This generates a 75% duty cycle digital clock to the output latch, and a 100KHz ramp voltage to be used in the feedback control.

FEEDBACK CONTROL

This block senses one of the various feedback methods to control the output duty cycle. It includes a current sense, a low pass filter, current amplifier, summing amp, and comparators. This block sums the analog ramp from the OSC, sense, and compensation node voltages into a comparator which triggers the falling edge of the PWM clock signal. This provides supply voltage compensation and load regulation to the power converter system.

OUT_DRV

A high speed, high current bipolar output stage capable of providing approximately 500 mA sink and 250 mA source current to charge and discharge the gate of a large power FET. It is understood that the total delay from the comp pin to the output pin should be about 100 ns.

Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Supply Voltage (Low Impedance Source)		V_{DD}	13	V
Supply Current (High Impedance Source)		I_{DD}	15	mA
Output Peak Current		I_{OUT}	600	mA
REGULATOR CURRENT		I_{REG}	10	mA
Continuous Power at 25° C	8L SOIC	P_D	750	mW
	8L PDIP		1000	mW
Junction Temperature		T_J	150	°C
Storage Temperature		T_{STG}	– 65 to 150	°C
Lead Temperature, Soldering 10 Seconds		T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

Over full junction temperature range of 0-105°C. Ambient temperature deratings will bepend on power dissipation and package thermal characteristics. Vdd = 12V, OV = 0V, CSNS = 0V. Cload = 1800pf, Creg = 100nf (AVVD to GND) unless otherwise stated. To start chip, Vdd must be raised above UVLhigh.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Startup Current	I_{DDO}	UVL_{HIGH} Threshold		64	100	µA
Supply Current	I_{DD}	No Load	1	2	4	mA
Startup Threshold	UVL_{HIGH}	AS998 AS998A	9 9.5	10 10	11 10.5	V V
UVL off Threshold	UVL_{LOW}		7.6	8	8.4	V
Bias Current at POS	V_{CLAMP}	I_{DD} = 10mA No Load	13	14	14.7	V
Int. Regulator Voltage	V_{REG}	I_{REG} = 1mA	5.5	6.25	7.0	V

Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Mean Period	T_{OSC}	8.4V < V_{DD} < 13.3V ; 15 cycle average - AS998 8.4V < V_{DD} < 13.3V ; 15 cycle average - AS998A	7.3 8.1	9.3 9.3	11.7 10.7	µs µs
Modulation Repetition Rate	T_{REP}			15		cycles
Peak-to-Peak Modulation	T_{DEV}	Peak-to-Peak change in period	13.7	16.5	23	%
Max. Duty Cycle	D_{MAX}		70	75	78	%

Error Amplifier

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FB Divider R	RFB			100		kΩ
V_{DD} Regulation Point	VDD_{REG}		11.4	12	12.6	V
FB Threshold	V_{REF}	COMP = FB, V_{DD} =12V	2.37	2.5	2.62	V
Gain (DC)	AV_{OL}	No load on COMP		85		dB
Gain-Bandwidth Product	GBP	No load on COMP		10		MHz
COMP Output High	V_{COMPH}	FB = 2V	4.5			V
COMP Output Low	V_{COMPL}	FB = 3V		100	250	mV
COMP Source Current	I_{COMPH}	COMP = 3V, FB = 2V	25	50	100	µA
COMP Sink Current	I_{COMPL}	COMP = 1V, FB = 3V	25	300	500	µA

Current Sense Comparator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Scaling of COMP		to CSNS input		0.4		
AC Input Impedance	R_{CSAC}	Fin ≥ Fco		100		kΩ
Input Filter	F_{CS}	Time Constant		320		ns
Prop. Delay to Output	tpd1			700		ns

Electrical Characteristics (cont.)

Over Current Comparator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Comparator Threshold	V_{CSTH}	COMP = 1V, FB = 3V		1.25		V
Propagation Delay to Output	tpd2	FB = 2, V_{CS} step to 1.65V, from 50% point on CSNS input to 90% point on output H to L transition		100	150	ns

Over Voltage Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OV V_{DD} Threshold	VDD_{OV}	Forcing VDD pin	13	14	14.7	V
OV Threshold	V_{OV}	Forcing OV pin		3.5		V
OV Latch State Low	OV_{RN}	OV = Reg - 1V, Equiv. R to Reg	4	8	16	kΩ
OV Latch State High	OV_{RP}	OV = 1V, Equiv. R to Gnd	4	8	16	kΩ
OV Hi Impedance Pull-up	OV_{HI}	OV = 1V, I_{DD} = 10mA		0.3	1	µA
OV Unlatch Threshold	VDD_{UL}	VDD dropped until latch fails	4.75	5	5.25	V

Output

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max. “Off State” Voltage	V_{OFF}	I_{OUT} = 100µA			1.7	V
Output Rise Time	tr	T = 25°C, 10% - 90%	170	250	290	ns
Output Fall Time	tf	T = 25°C, 10% - 90%	140	210	240	ns